REMARKS

Applicants have carefully reviewed the Office Action dated July 1, 2004. Claims 1-6 are pending in this application. Claims 8-13 are withdrawn from this application. Applicants have amended Claims 1 and 3 to more clearly point out the present inventive concept. Reconsideration and favorable action is respectfully requested.

Claims 1-6 stand rejected under 35 U.S.C. §102(b) as being anticipated by *Allen et al.* This rejection is respectfully traversed with respect to the amended claims.

As stated in the previous response, Applicants' present inventive concept is directed toward the interface of input/output pins with a re-configurable processor. The re-configurable processor is reconfigured to provide different functionalities such that this functionality can be "altered" by the reconfiguration of the integrated circuit. The input/output pins associated with each of the configurations can be selected in a desired order. This configuration information is stored in non-volatile memory on -chip. The claims have been amended to more clearly define that the functionality of each of the functional blocks is associated with the input/output pins by the configuration information. Each of these functional blocks has associated therewith a requirement for a defined number of input/output pins. The integrated circuit is designed such that it has more functionality than available pins and, as such, not all of the functional blocks can be selected at any one time. The claims have been amended to clarify this aspect.

The *Allen* reference discloses only that an on-board memory can contain configuration information to allow input/output pins to be selected for connection to signal inputs to the microprocessor core logic or to signal outputs from the microprocessor core logic. This is nothing more than a multiplexing configuration. There is no disclosure as to the fact that there are multiple functions that are provided on the chip that each require a certain number of pins to achieve that functionality and that the number of functional block and the associated requirement for input/output pins in total exceeds that of the available input/output pins. As such, Applicants believe that the *Allen et al* reference does

not anticipate or obviate Applicants' present inventive concept, defined by the amending claims, and, therefore, respectfully requests withdrawal of the 35 U.S.C. §102(b) rejection with respect thereto.

Claims 1-6 have also been rejected under 35 U.S.C. §103(a) as being unpatentable in view of *Cheung et al*. This rejection is respectfully traversed with respect to the amended claims.

As noted in the previous office action, the *Cheung et al* reference does not disclose the use of on-board memory. Nor does *Cheung et al* disclose the combination of the on-chip memory, the multiple functional blocks with the requirement for a number of pins. *Cheung* does not provide such combination and, as such, Applicants believe that the claims as amended are not anticipated or obviated by the *Cheung, et al* reference. Therefore, Applicants respectfully request withdrawal of the 35 U.S.C. §103(a) rejection with respect to the rejected claims.

Applicants have now made an earnest attempt in order to place this case in condition for allowance. For the reasons stated above, Applicants respectfully request full allowance of the claims as amended. Please charge any additional fees or deficiencies in fees or credit any overpayment to Deposit Account No. 20-0780/CYGL-25,768 of HOWISON & ARNOTT, L.L.P.

Respectfully submitted,
HOWISON & ARNOTT, L.L.P.
Attorneys for Applicants

Gregory M. Howison
Registration No. 30,646

GMH/yoc/cr

P.O. Box 741715
Dallas, Texas 75374-1715
Tel: 972-479-0462
Fax: 972-479-0464
October 1, 2004